

Transceiver

100G CWDM4 (TOSA M-LD) OWOT-100M-11



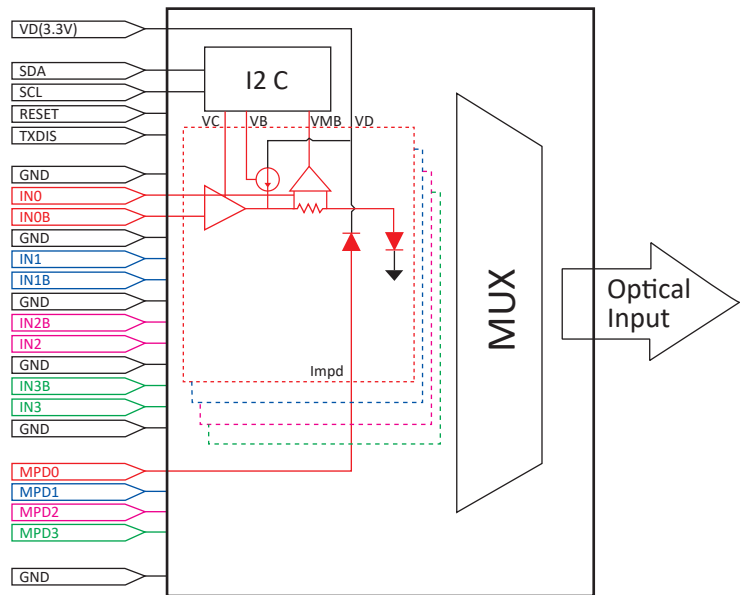
Key Features

- Up to 25.78125 ±100 ppm Operation (NRZ)
- Direct Modulation Laser (DML) Base Quad TOSA for CWDM4
- Useable with M37049G-16 CDR
- Integrated LDD
- 2 Wire Communication (Up to 400 kHz)
- CWDM4 Optical MUX Integrated
- Pigtail with LC Connector
- SMT Style for Electrical RF Signals

Applications

- CWDM4 MSA
- QSFP28/CFP2/CFP4 Transceiver Modules
- On Board Optics

Modular Block Diagram



Optical and Electrical Characteristics

T_c = 0°C to 80°C, (unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.
Bit Rate		NRZ, each lane		25.781 Gb/s	
Operational Case Temperature	T _c		0°C	25°C	80°C

Laser

Peak Wavelength for L0	L ₀ ¹	for L0	1264.5 nm	1271 nm	1277.5 nm
	L ₁ ¹	for L1	1284.5 nm	1291 nm	1297.5 nm
	L ₂ ¹	for L2	1304.5 nm	1311 nm	1317.5 nm
	L ₃ ¹	for L3	1324.5 nm	1331 nm	1337.5 nm
Average Output Power	P _f	each lane ¹	-6.5 dBm	0.0 dBm	2.5 dBm
Total Average Launch Power	P _T				8.5 dBm
Optical Modulation Amplitude	POMA _I	each lane ¹	-4 ² dBm	-0.65 dBm	2.5 dBm
Extinction Ratio ¹	ER		3.5 dB		
Optical Return Loss Tolerance	ORL				20 dB
Transmitter Reflectance	T _R				-12 ³ dB
Side-mode Suppression Ratio	SSR		30 dB		
Transmitter and Dispersion Penalty	TDP	each lane, SMF = 2 km			3.0 ⁴ dB
Transmitter eye mask definition (X1, X2, X3, Y1, Y2, Y3) ^{1, 4, 5}		4 th Bessel		Refer to Figure1 (0.31, 0.4, 0.45, 0.34, 0.38, 0.4)	
Mask Margin	MM	5E-5		25%	

Monitor PD

Monitor PD Current	I _{mpd}	P _f = 0 dBm	TBD		TBD
Reverse Voltage	V _{rp}	P _f = 0 dBm	1.5 V		

Optical and Electrical Characteristics

T_c = 0°C to 80°C, (unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.
I2C / Driver					
Supply Voltage	V _D		2.97 V	3.3 V	3.47 V
Supply Current	I _D			TBD	TBD
DML Bias Current	I _{BIAS}				70 mA
DML Bias Control Voltage	V _{B0~3}				2.5 V
Modulation Control Voltage	V _{C0~3}				2.5 V
Cross Point Control Voltage	V _{X0~3}				1.0 V
Data Input Amplitude	I _N	AC coupled	0.7 V _{ppd}		1.5 V _{ppd}
Input Logic Voltage High ⁶	V _{IH}	SDA, SCL, RESET, TXDIS	1.3 V	1.8 V	3.47 V
Input Logic Voltage Low ⁶	V _{IL}	SDA, SCL, RESET, TXDIS	0 V	0 V	0.4 V
Output Logic Voltage High ⁶	V _{OH}	SDA, I _{OH} = I _{OL} = 4 mA	1.5 V	1.7 V	1.92 V
Output Logic Voltage Low ⁶	V _{OL}	SDA, I _{OH} = I _{OL} = 4 mA		0 V	0.3 V
Total Power Dissipation	P _{total}			TBD	TBD

1: 25.8 Gbps, PRBS = 231-1.

2: Even if the TDP < 1.0dB, the OMA (min) must exceed this value.

3: Transmitter reflectance is defined looking into the transmitter.

4: TDP does not include a penalty for multi-path interference (MPI).

5: See mark in Figure 1.

6: See recommended circuit in Figure 2.

Figure 1. Transmitter Eye Mask

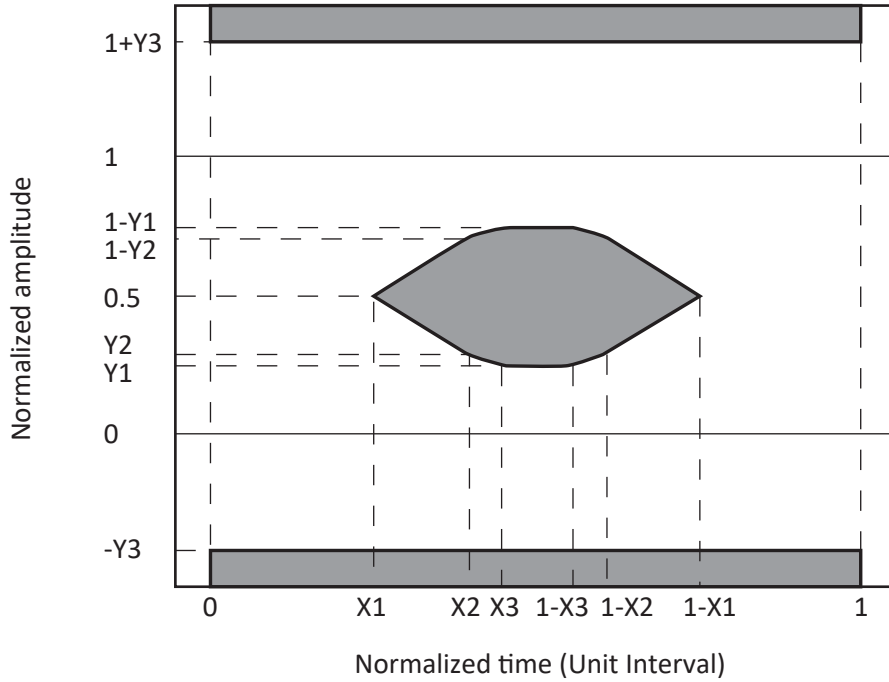
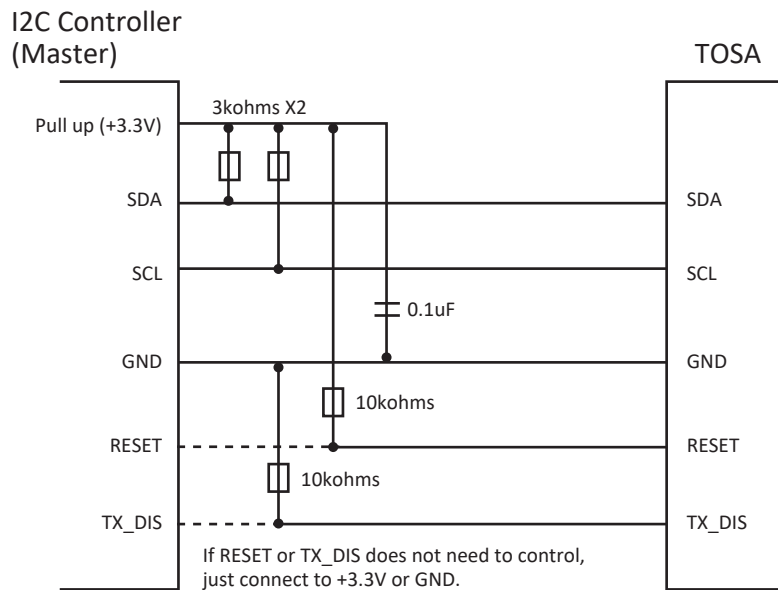


Figure 2. Recommended Circuit

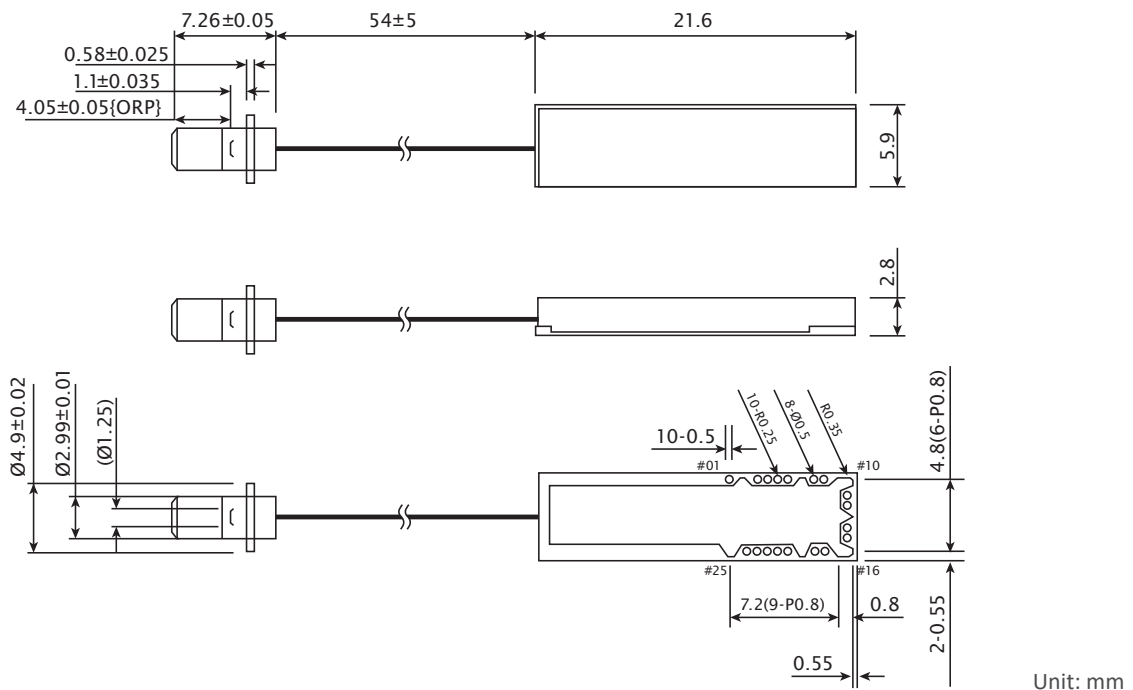


Absolute Maximum Ratings

T_c = 25°C, (unless otherwise specified)

Parameter	Symbol	Condition	Min.	Max.
Supply Voltage	VD		-0.3 V	3.6 V
Data Input Amplitude	IN0~3	AC coupled		2.5 Vppd
Monitor Photodiode Forward Current	Impd_f			10 mA
Monitor Photodiode Reverse Voltage			20 V	
Storage Temperature	Tstg		-40 degC	85 degC
Electrical Discharge Voltage(HBM)	VESD,HBM			TBD

Dimensions



Pin Configuration

Pin#	Symbol	Description	Pin#	Symbol	Description
1	N/C	No Connection	14	IN1	Positive data input for L1
2,7,10,13,16,19,25	GND	Ground	15	IN1B	Negative data input for L1
3	MPD0	Monitor PD anode for L0	17	INO	Positive data input for L0
4	MPD1	Monitor PD anode for L1	18	IN0B	Negative data input for L0
5	MPD2	Monitor PD anode for L2	20	SDA	Two-wire serial interface data
6	MPD3	Monitor PD anode for L3	21	SCL	Two-wire serial interface clock
8	IN3B	Negative data input for L3	22	TXDIS	Global power down for disable, active high
9	IN3	Positive data input for L3	23	VD	+3.3 Voltage Power Supply
11	IN2B	Negative data input for L2	24	RESET	Reset signal, active high
12	IN2	Positive data input for L2			

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